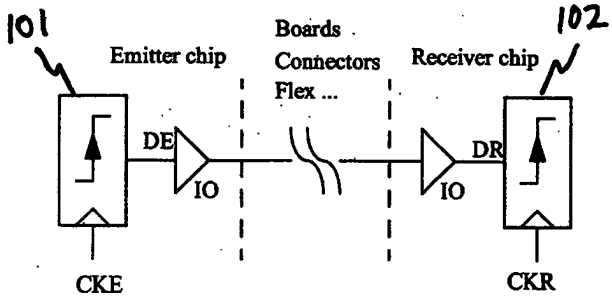

Figure 1

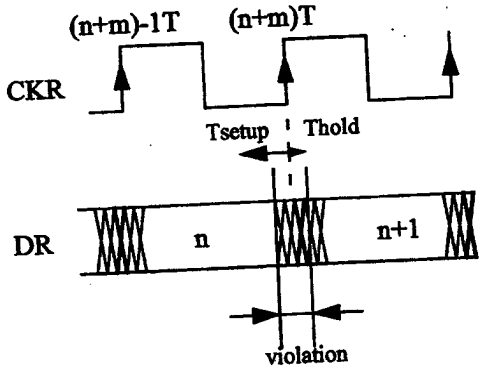

Figure 2

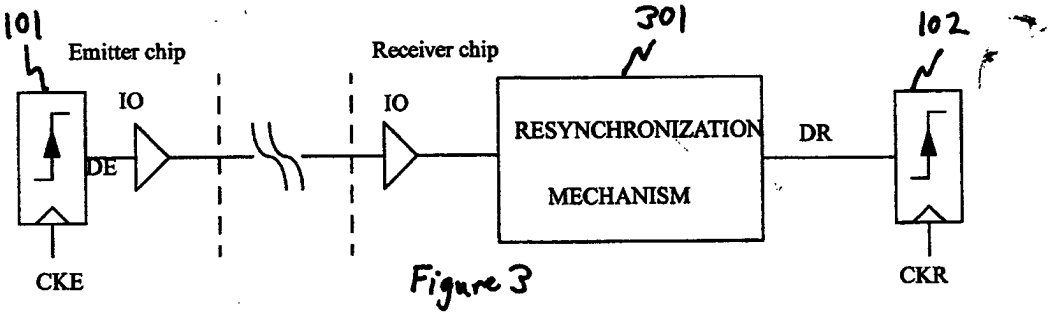

Figure 3

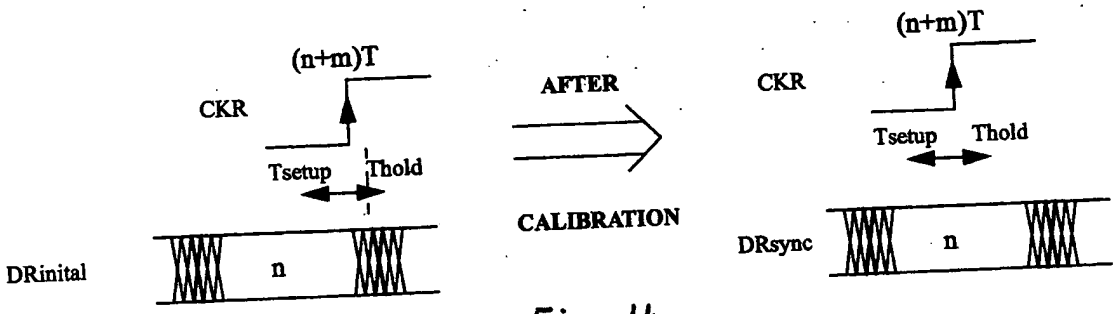

Figure 4

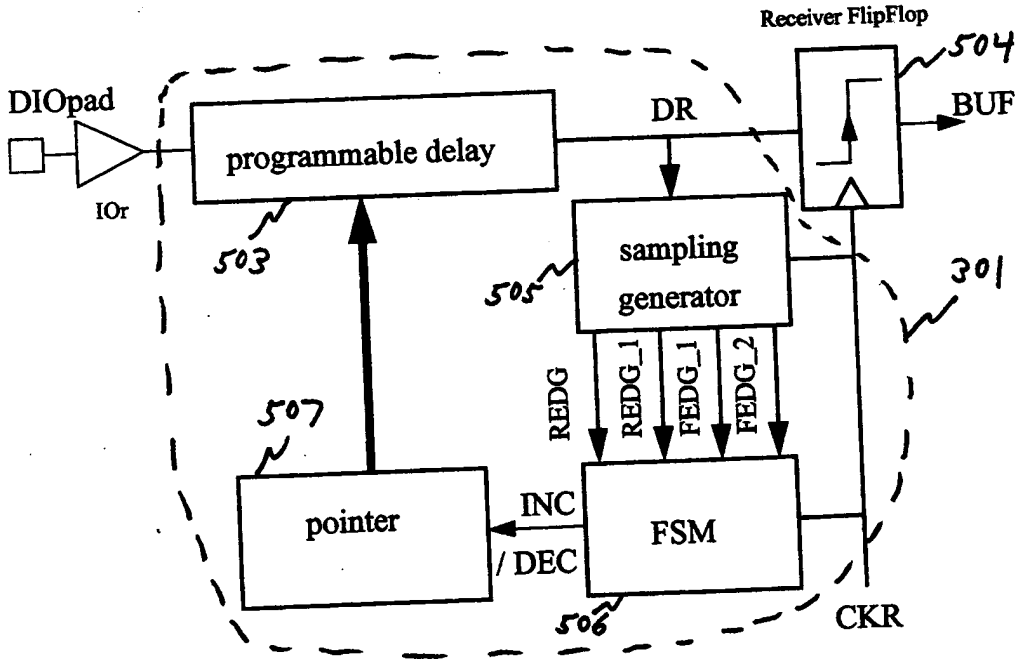

Figure 5

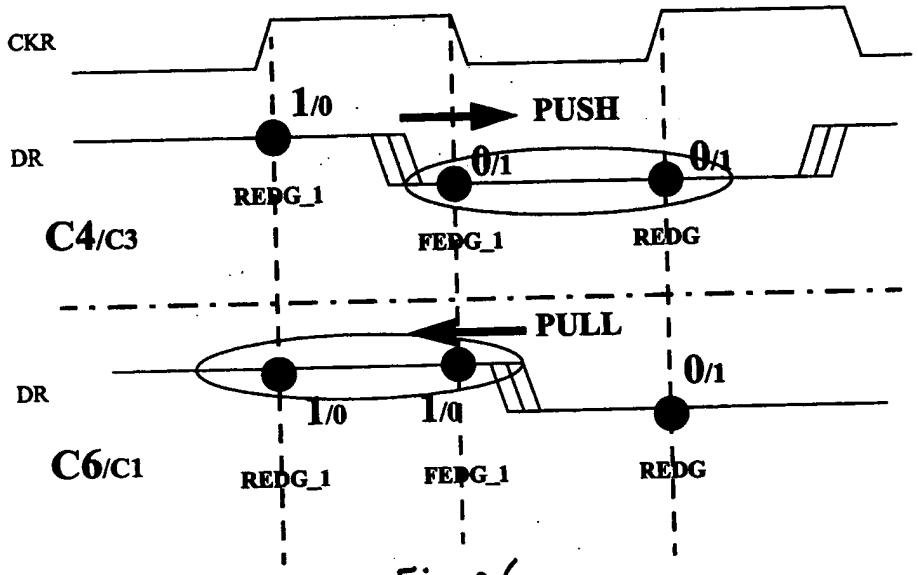

Figure 6

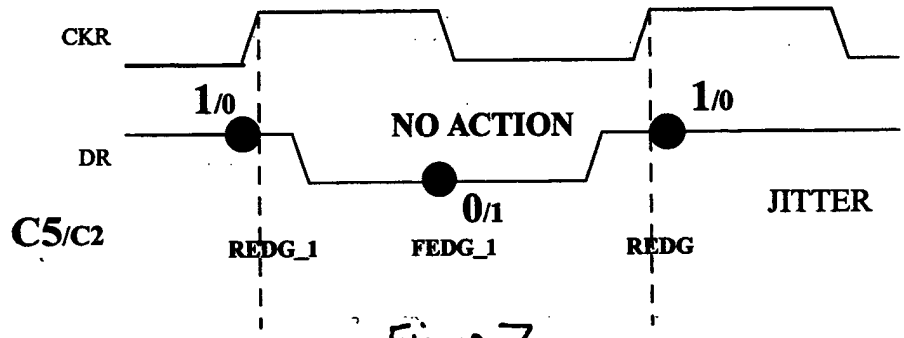

Figure 7

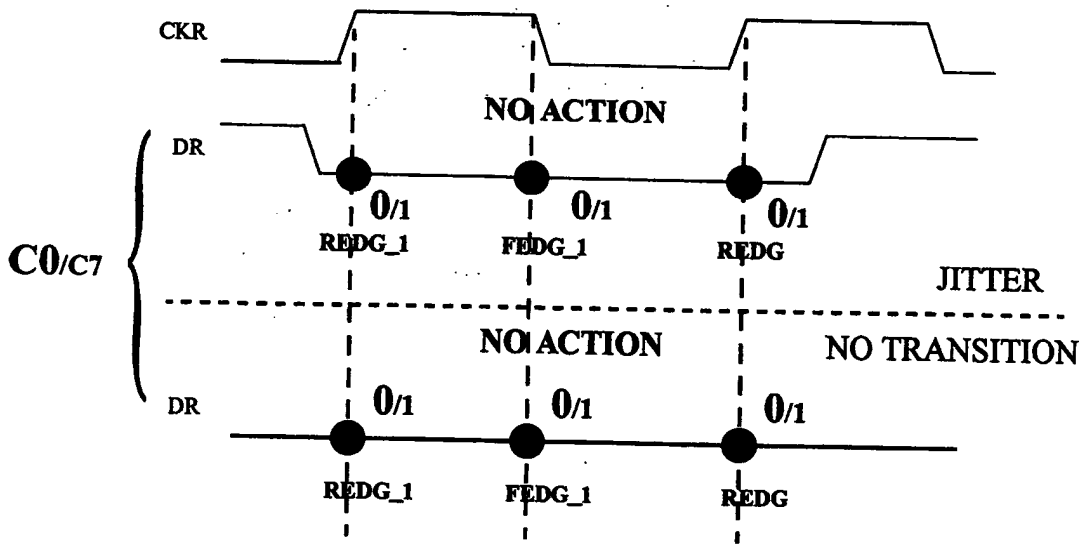

Figure 8

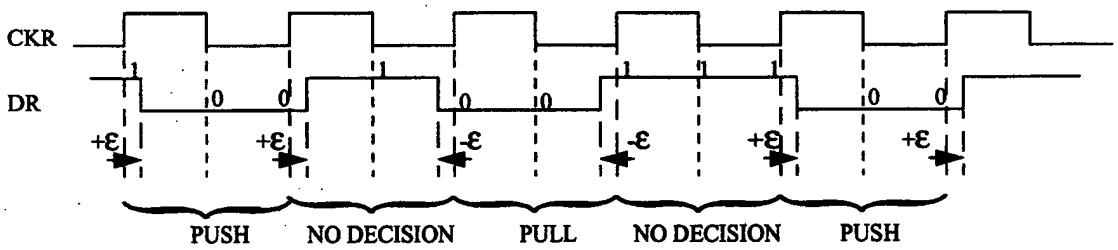

Figure 9

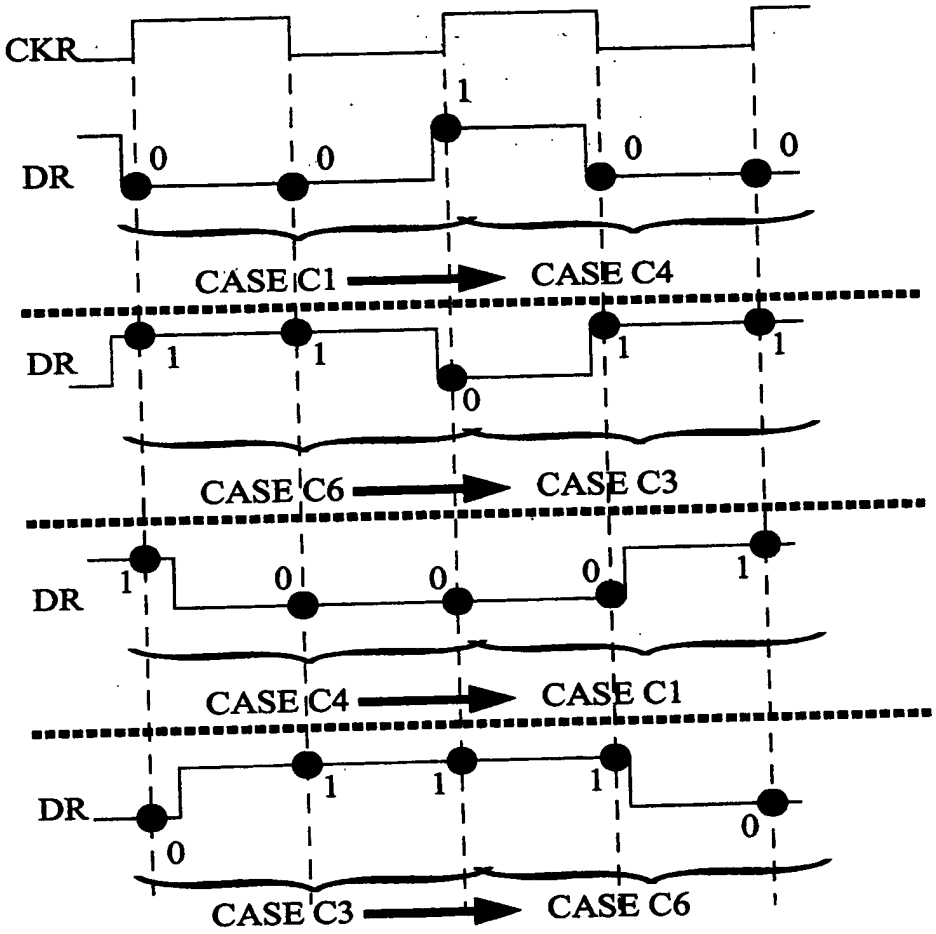

Figure 10

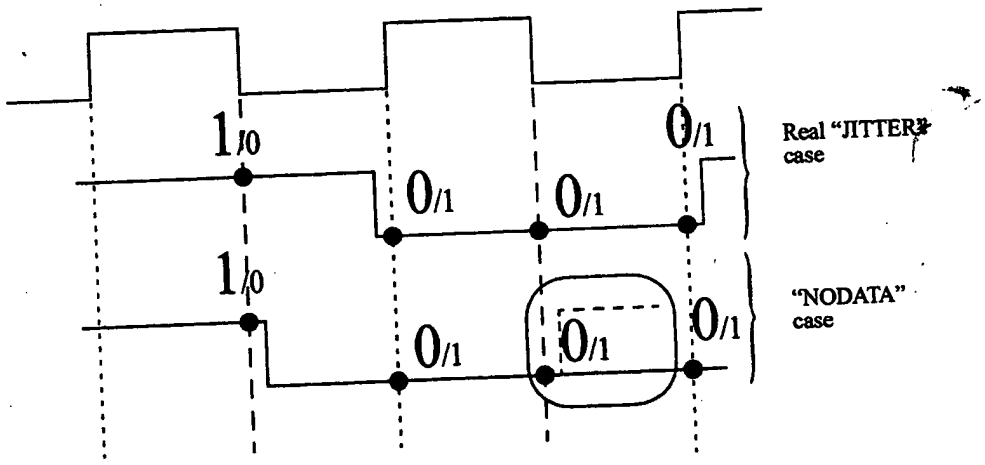

Figure 11

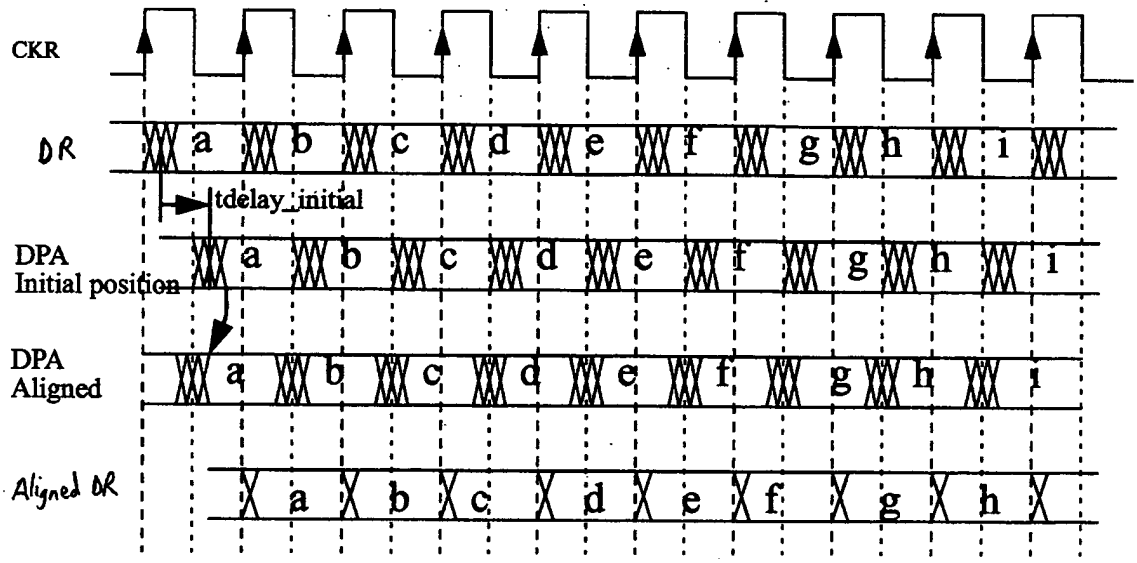

Figure 12

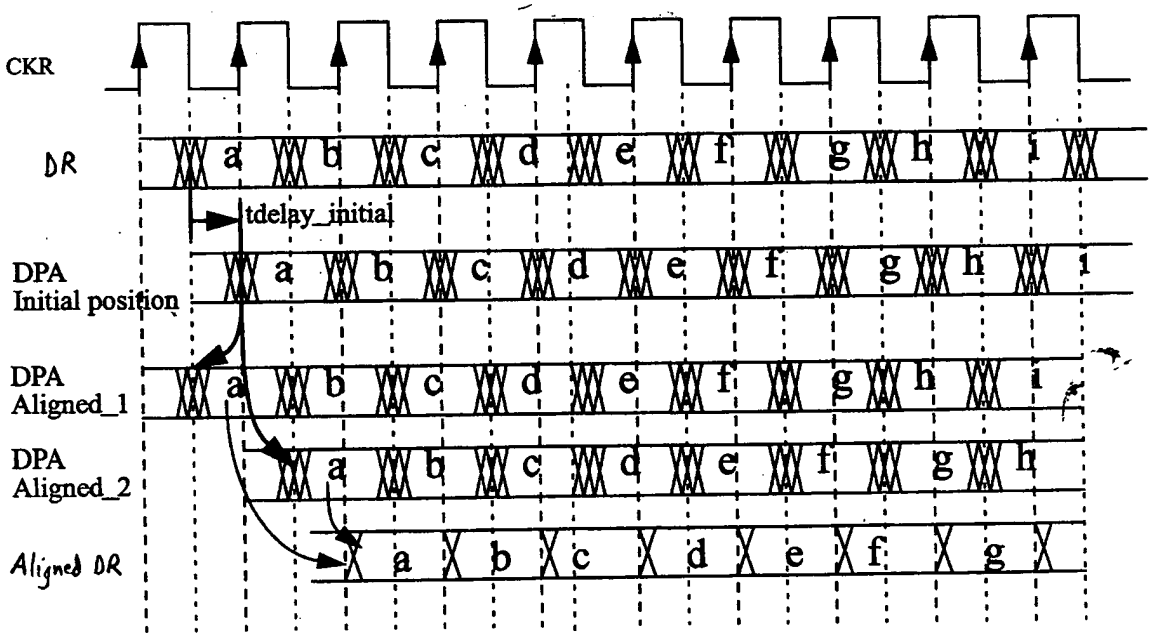

Figure 13

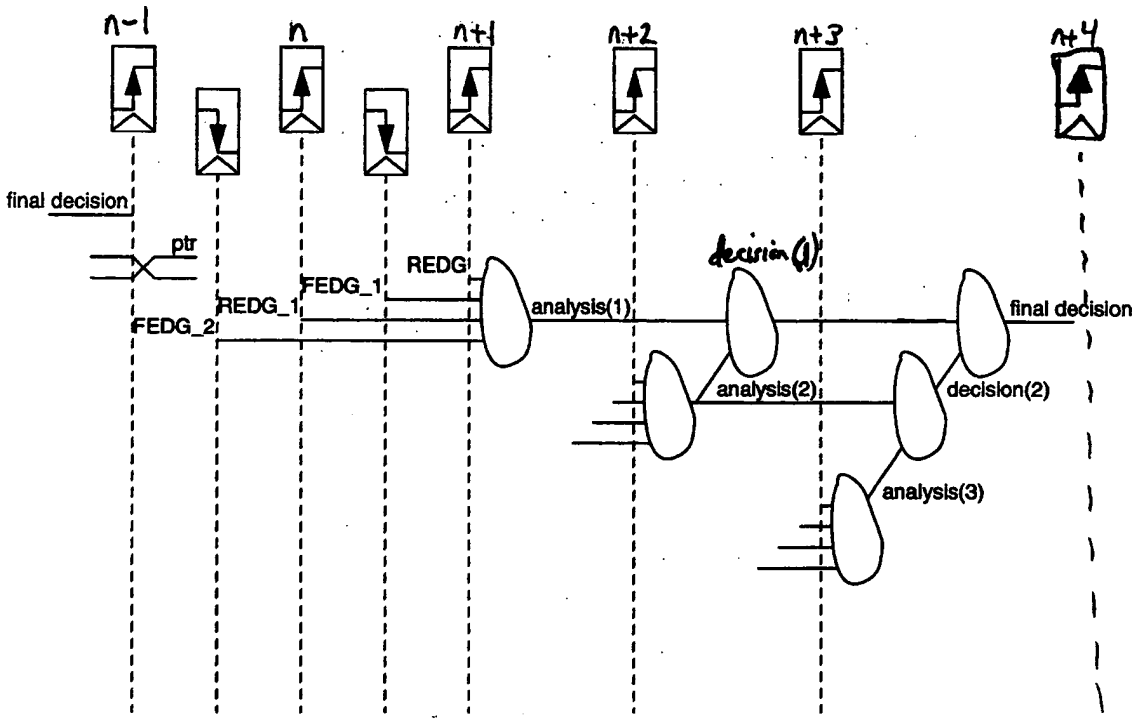

Figure 14

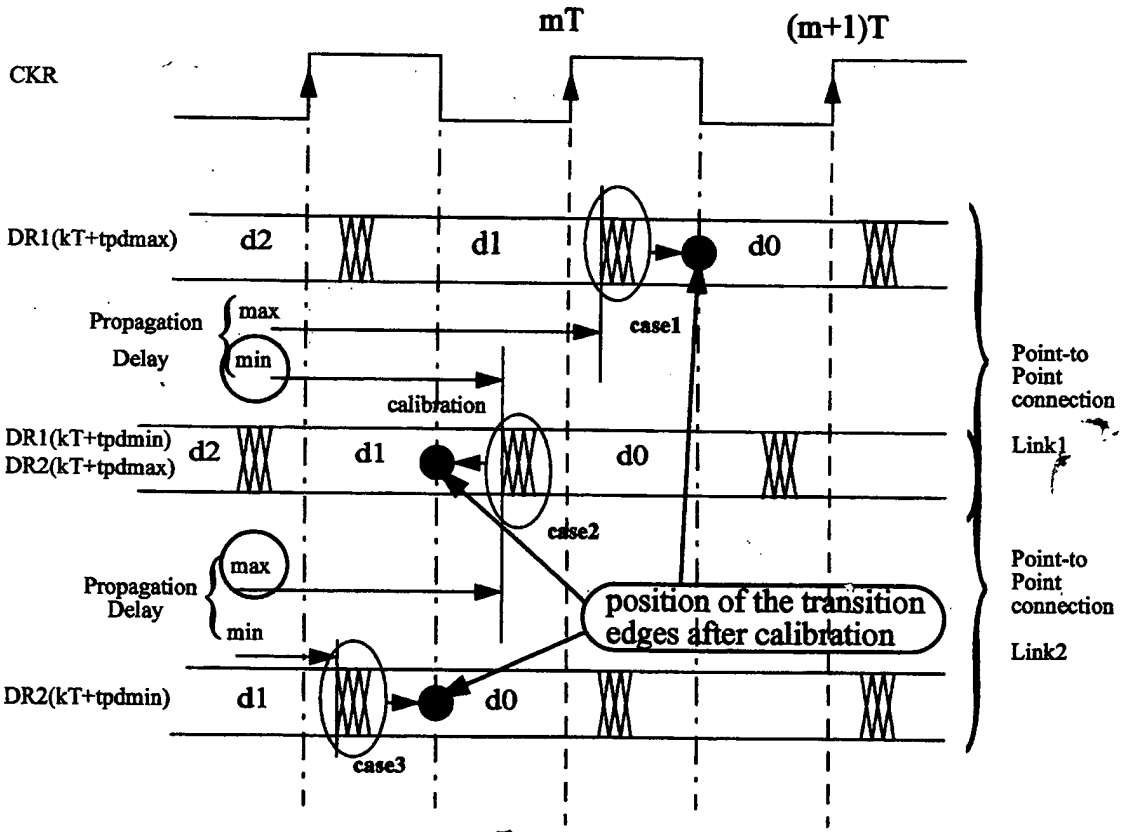

Figure 15

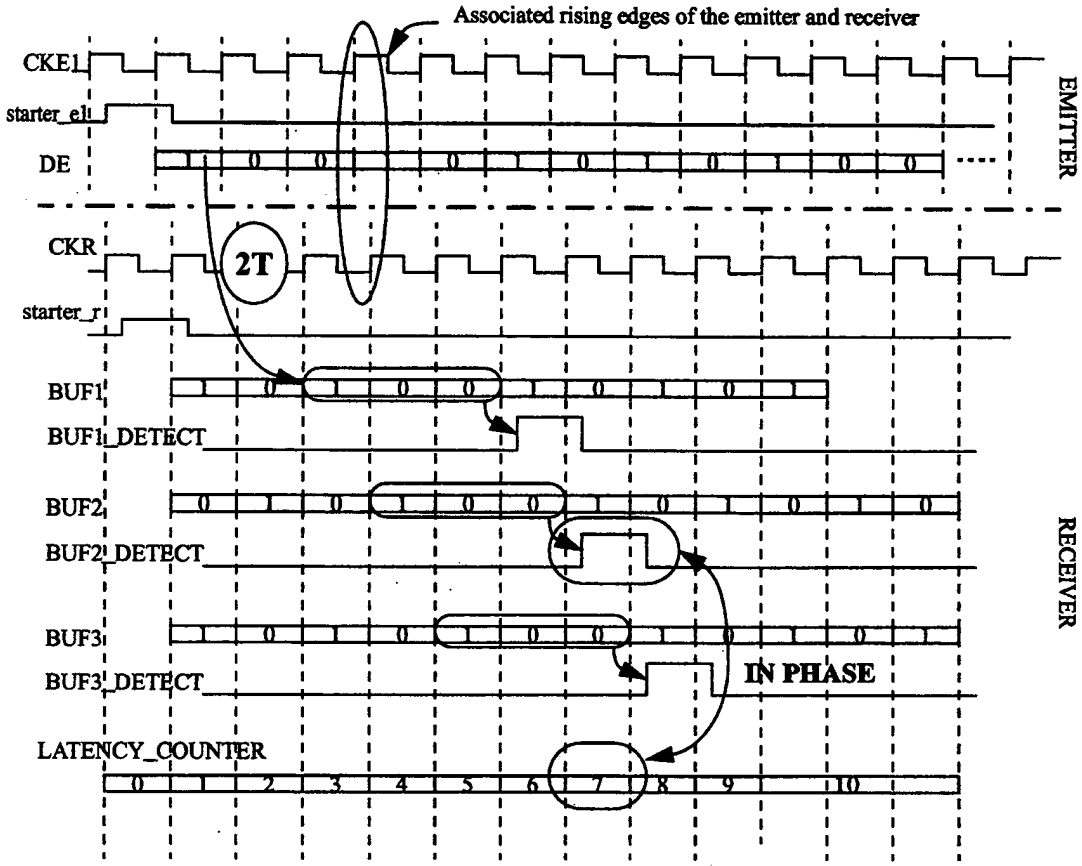
Associated rising edges of the emitter and receiver
CKE1
starter_e1
DE
EMITTER
CKR
2T
starter_r
BUF1
BUF1_DETECT
BUF2
BUF2_DETECT
BUF3
BUF3_DETECT
IN PHASE
LATENCY_COUNTER
RECEIVER

Figure 16

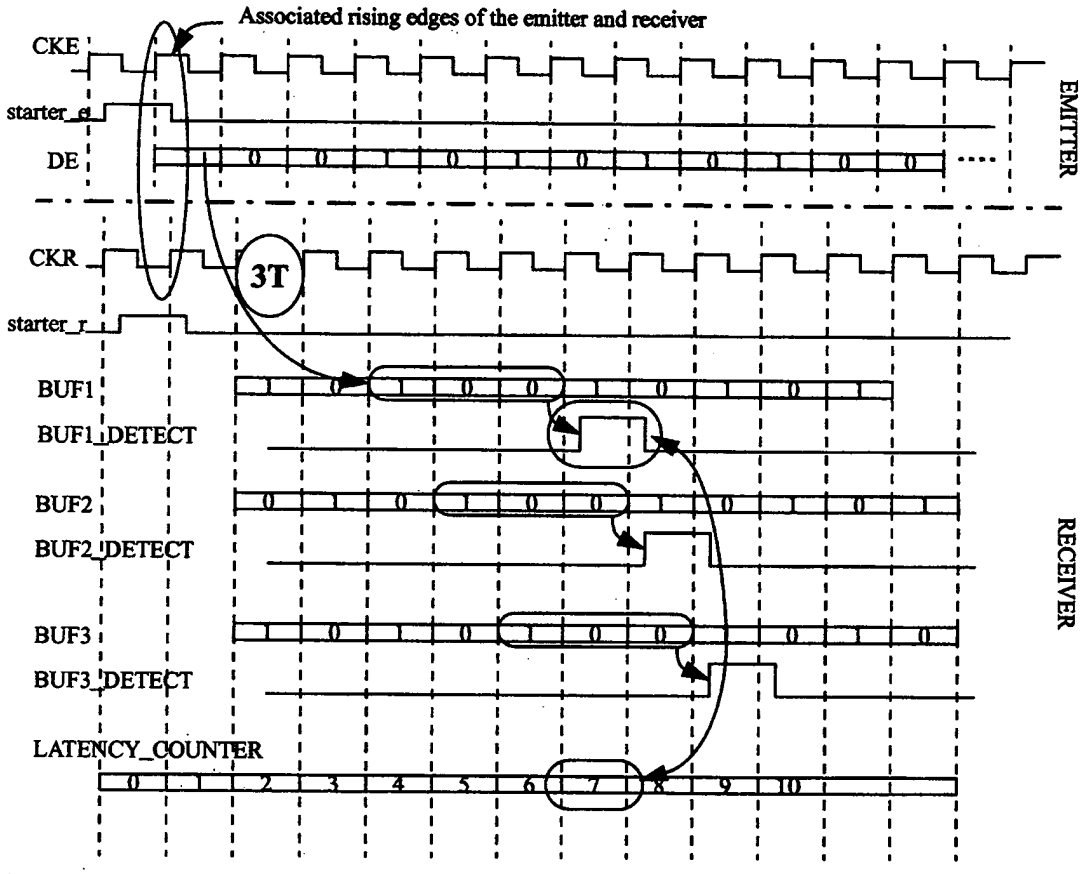
Associated rising edges of the emitter and receiver
CKE
starter_e
DE
EMITTER
CKR
3T
starter_r
BUF1
BUF1_DETECT
BUF2
BUF2_DETECT
BUF3
BUF3_DETECT
LATENCY_COUNTER
0 1 2 3 4 5 6 7 8 9 10
RECEIVER

Figure 17

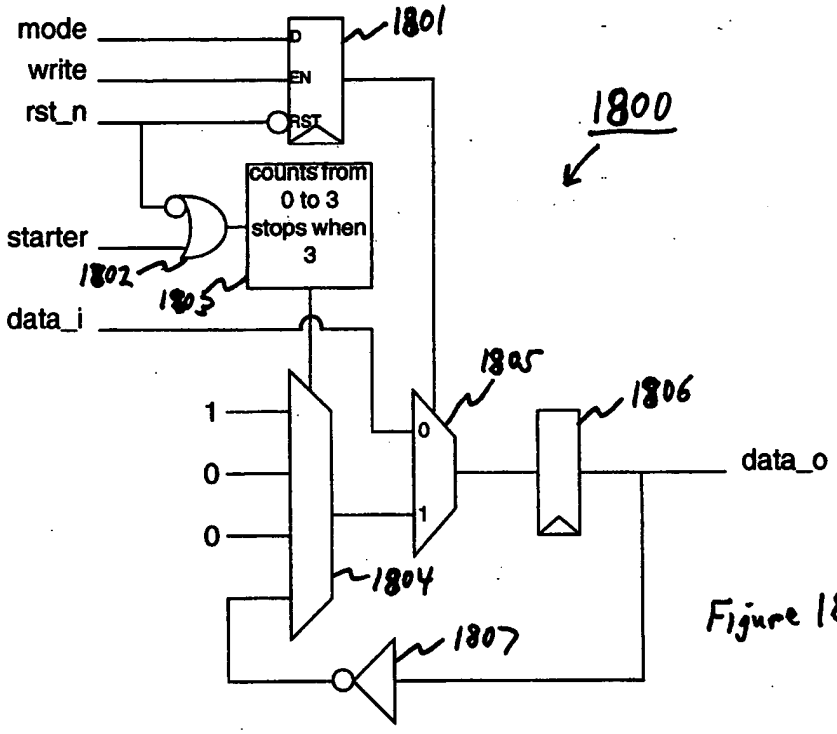

Figure 18

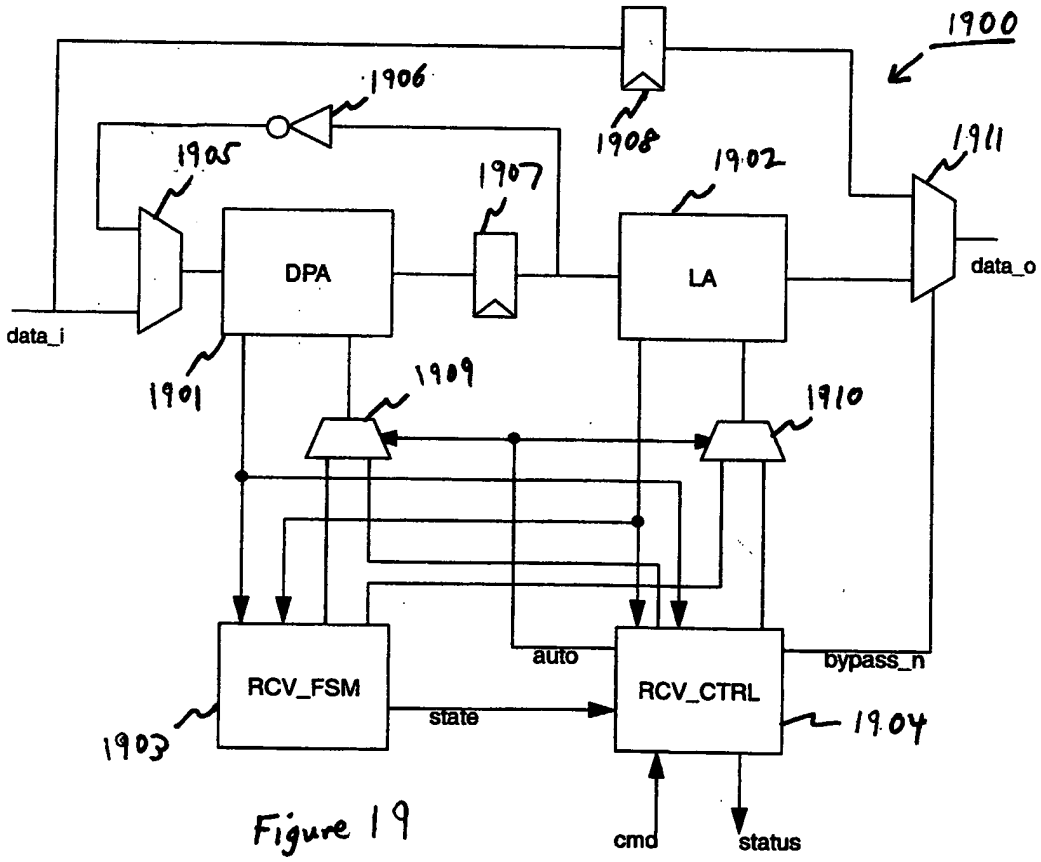

Figure 19

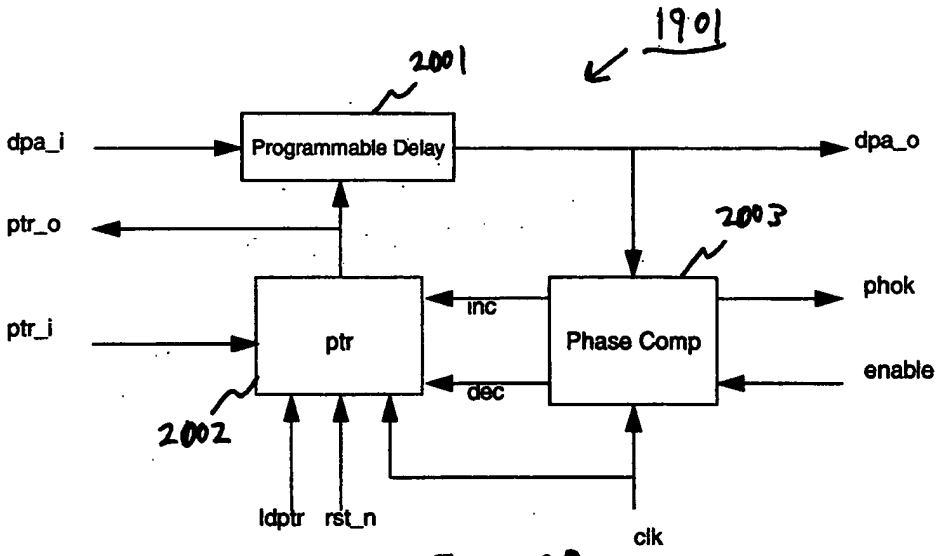

Figure 20

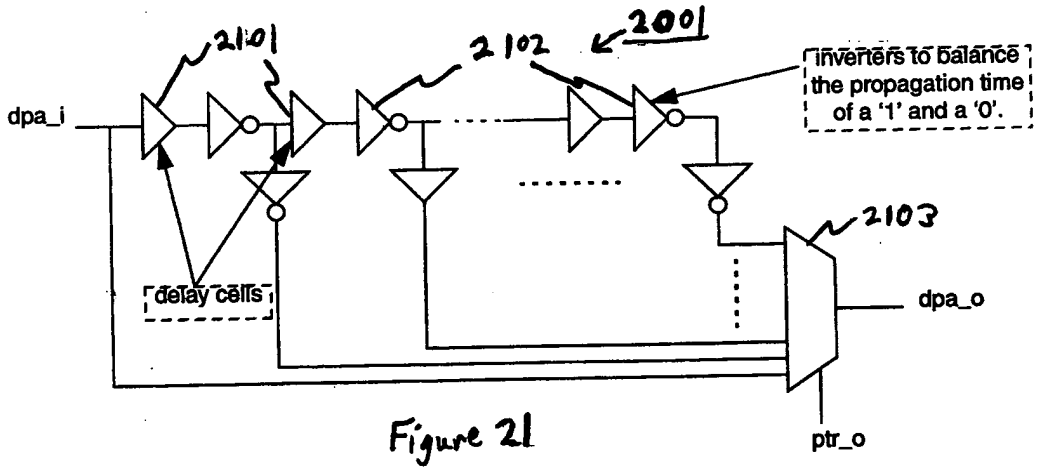

Figure 21

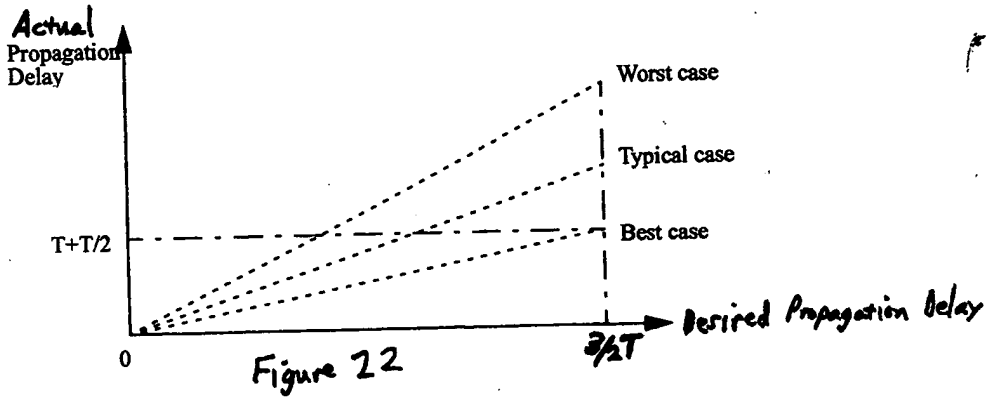

Figure 22

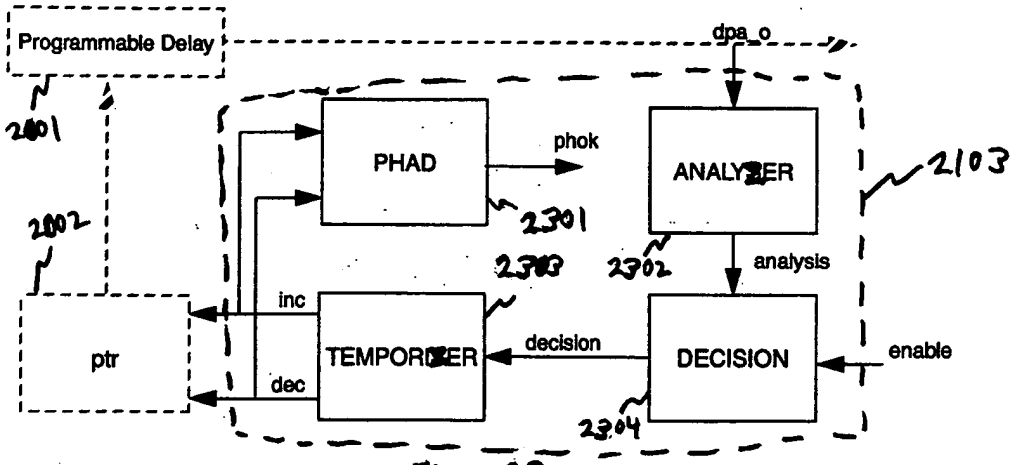

Figure 23

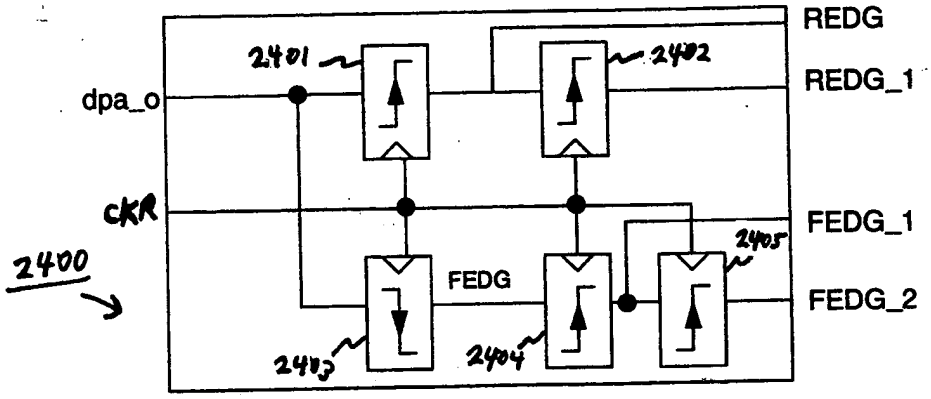

Figure 24

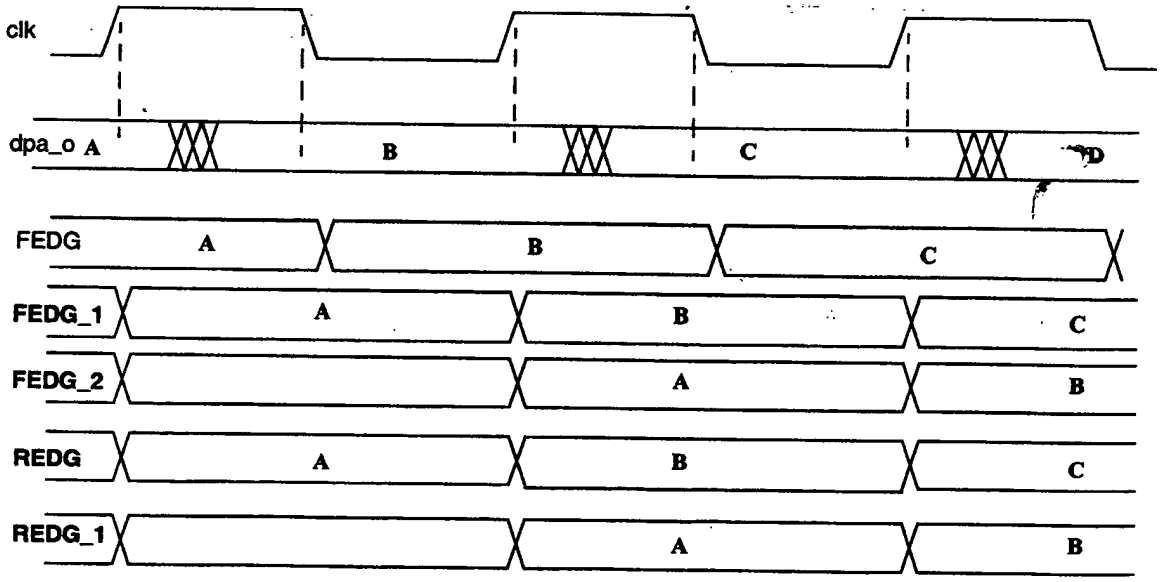

Figure 25

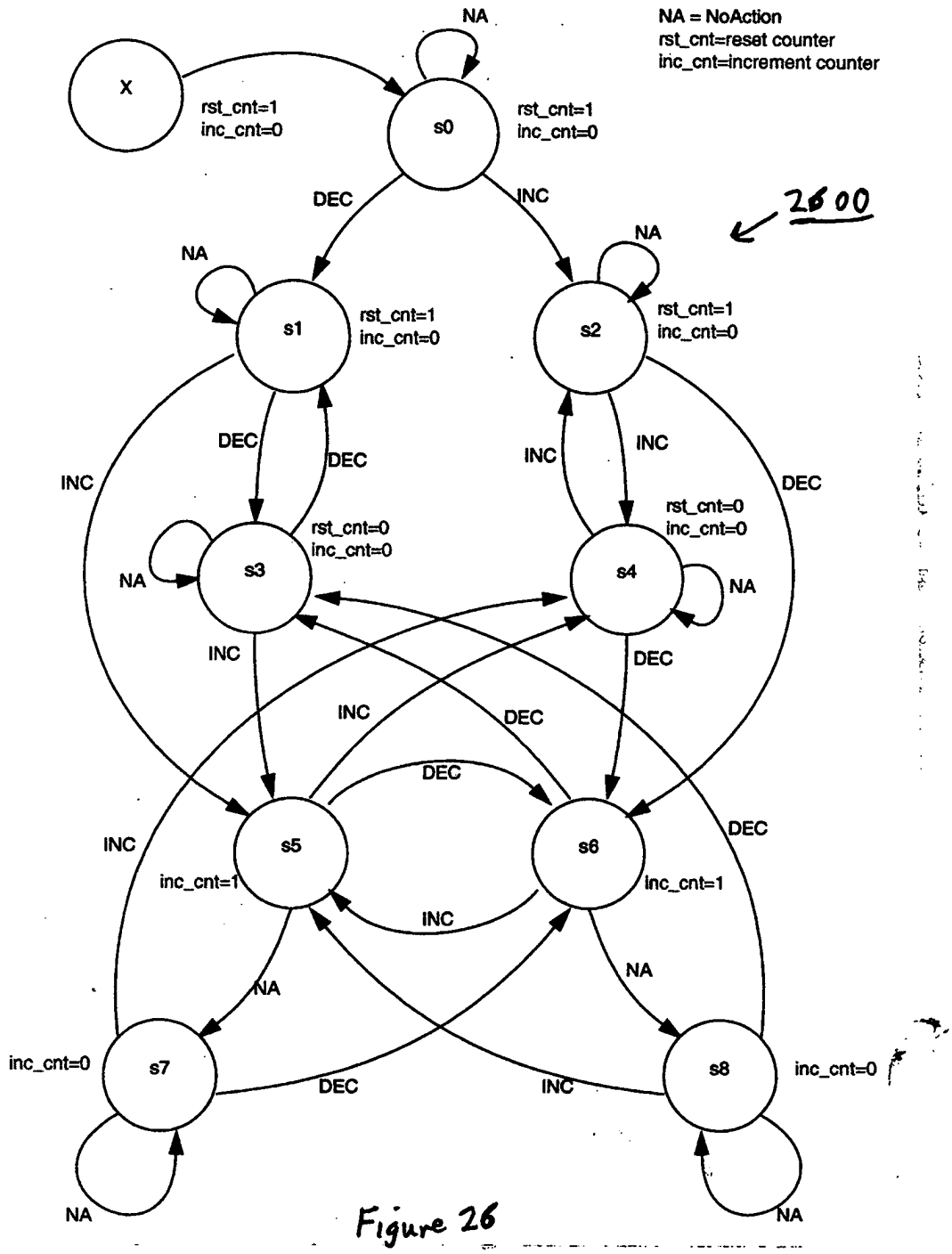
NA = NoAction
rst_cnt=reset counter
inc_cnt=increment counter
2600
X
s0
s1
s2
s3
s4
s5
s6
s7
s8
NA
rst_cnt=1
inc_cnt=0
rst_cnt=0
inc_cnt=0
inc_cnt=1
DEC
INC

Figure 26

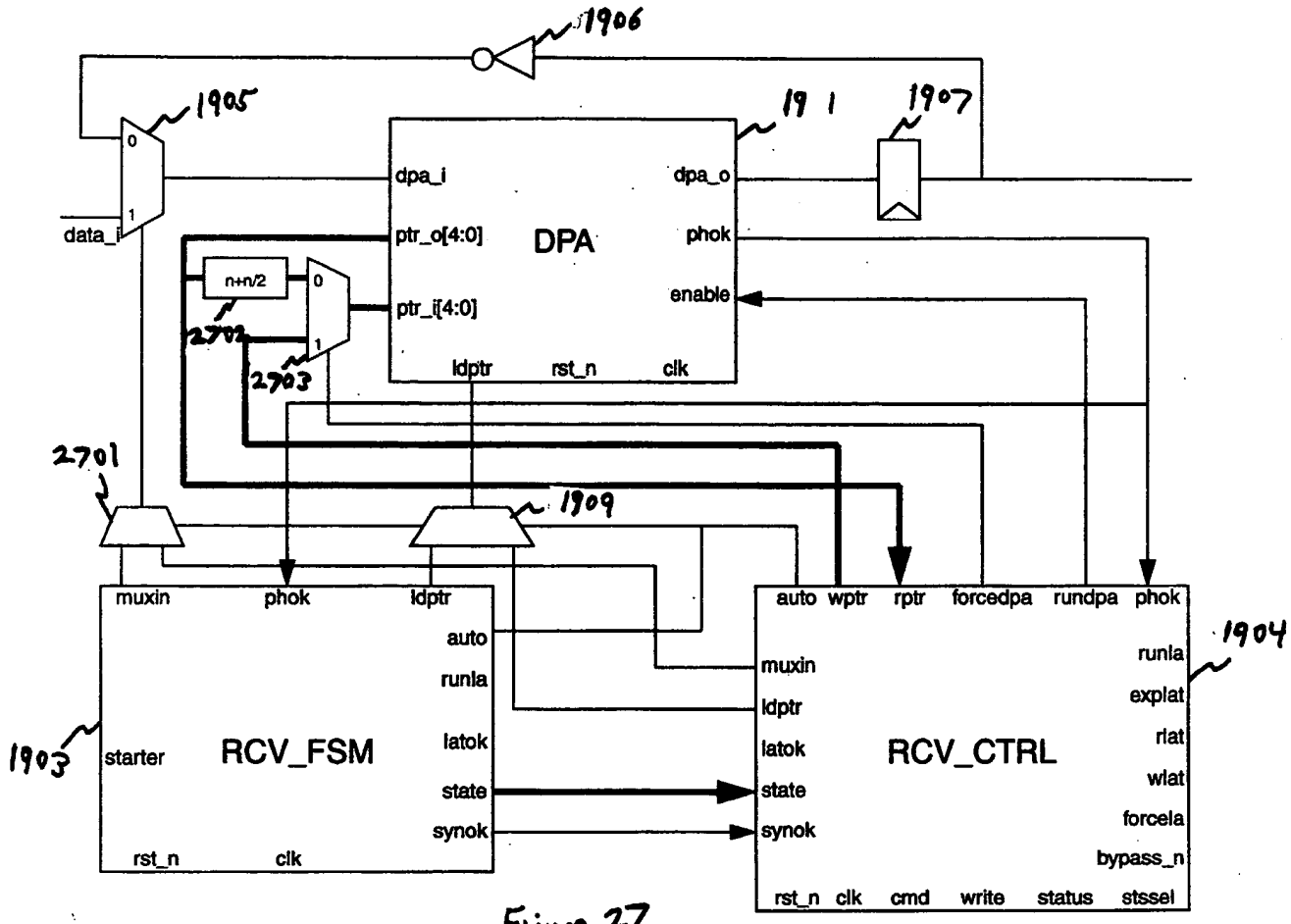

Figure 27

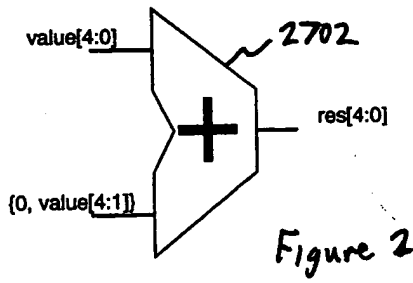

Figure 28

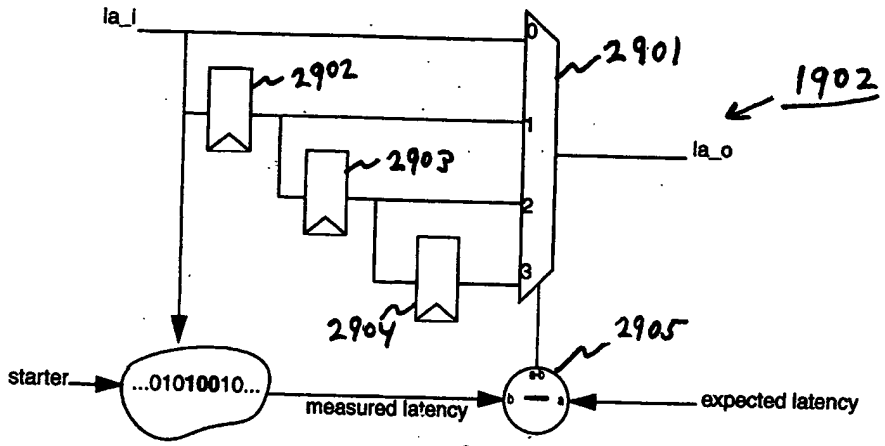

Figure 29

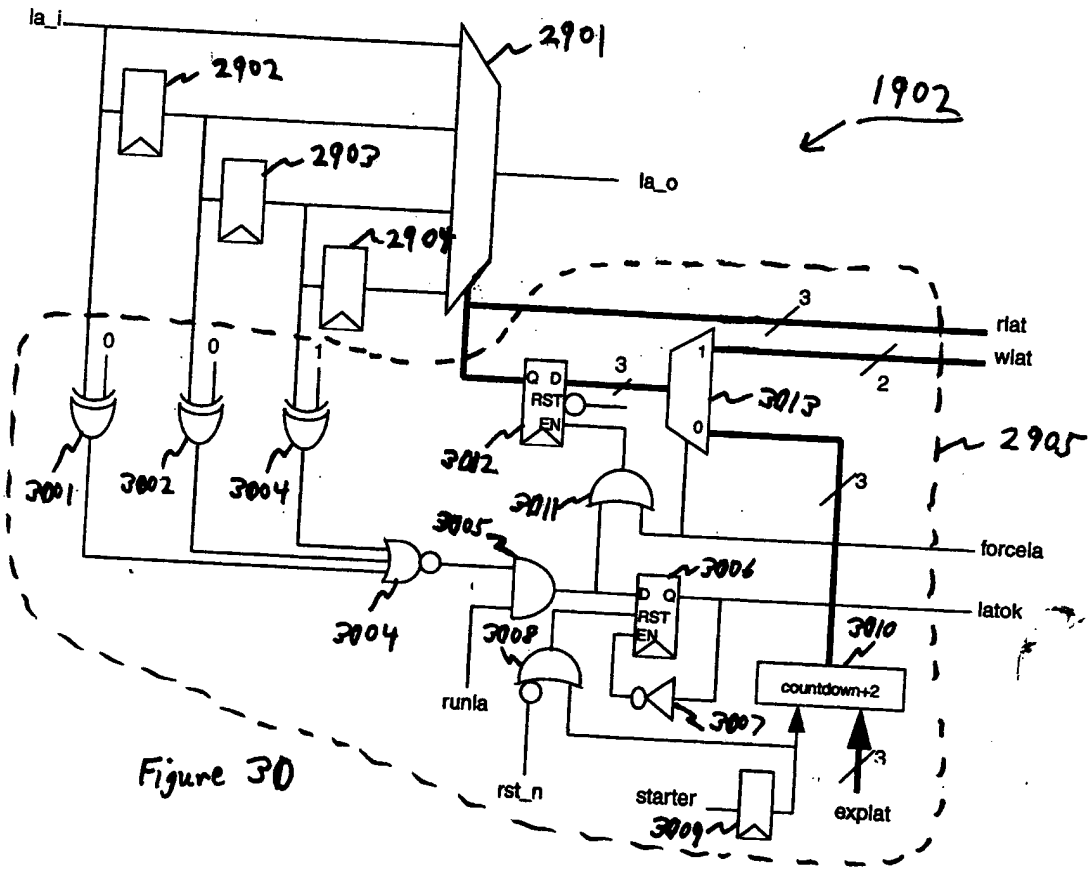

Figure 30

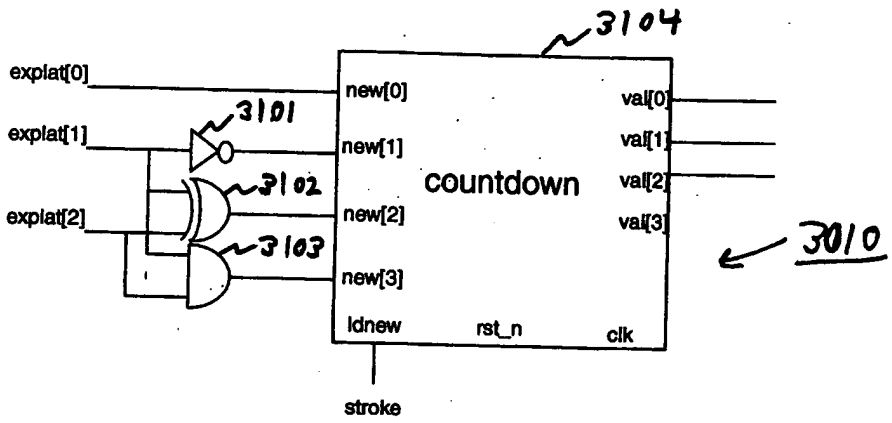

Figure 31

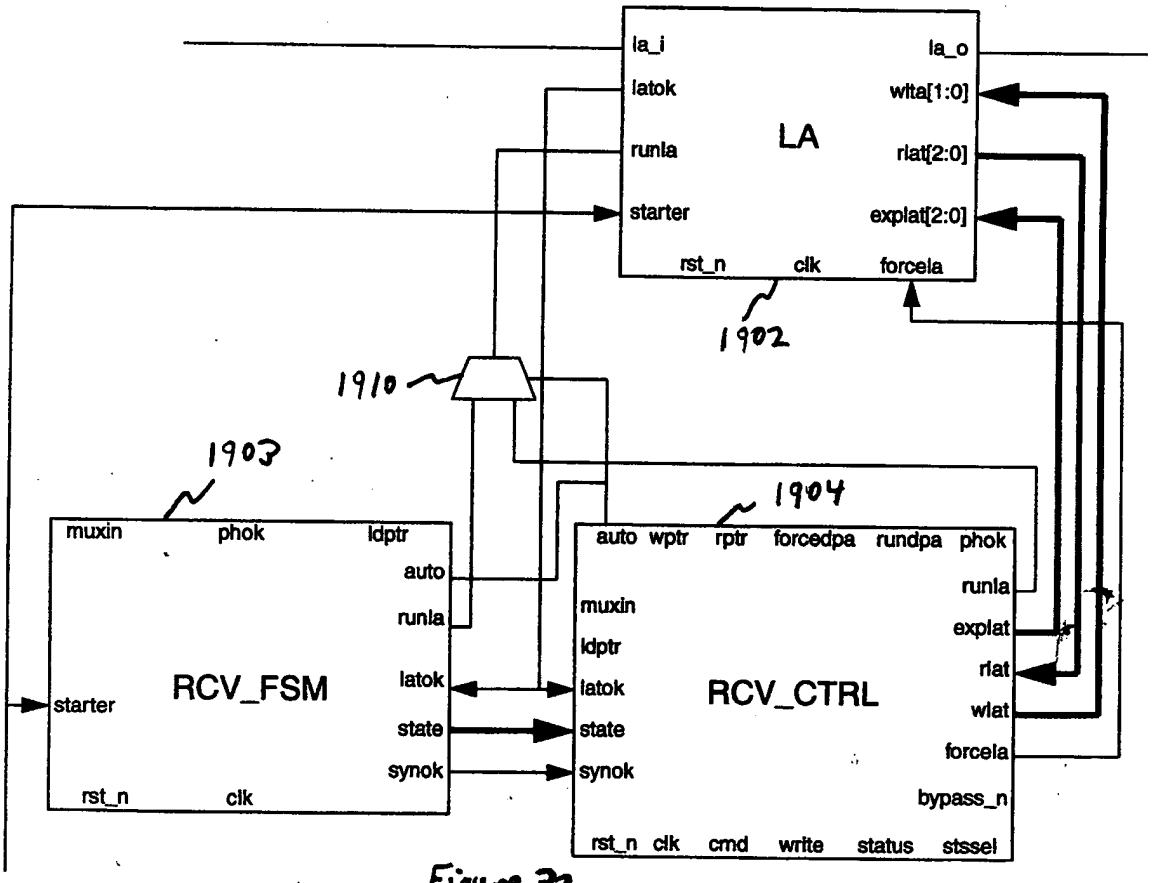

Figure 32

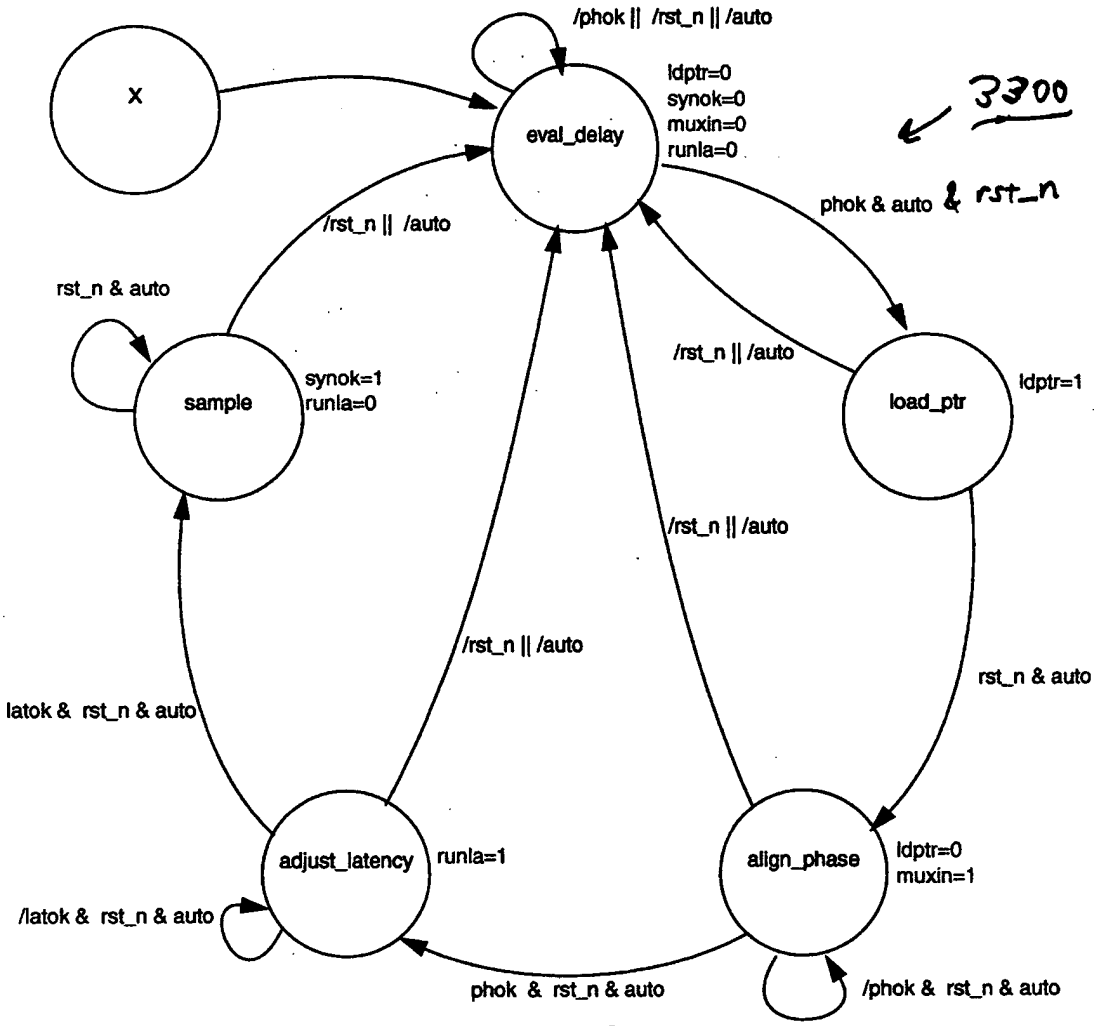

Figure 33

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO

Figure 34

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
XXXXXXXXXX		SYNOK	LATOK	PHOK	FSM_STATE			RLAT			RPTR				

Figure 35

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Figure 36

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	X	0	**Expected latency**			X	0	X	X	X	X	X	X	X	1

Figure 37

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	0	1	1	0	0	0	0	0	0	0

Figure 38

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	1	0	0	0	0	0	0	0	0	0

Figure 39

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	0	0	1	X	X	X	X	X	1	0

Figure 40

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	1	0	0	X	X	X	X	X	0	0

Figure 41

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	1	0	Expected latency			1	0	0	X	X	X	X	X	0	0

Figure 42

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	1	0	0	X	X	X	X	X	0	0

Figure 43

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	1	0	1	1	1	1	0	0	X	X	X	X	X	0	0

Figure 44